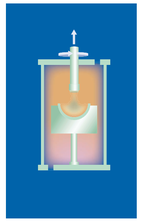
The Making of a Microchip

1

Quartz or Sand (SiO_2) is processed to form pure silicon, which is then melted in a quartz crucible.

A seed crystal is lowered into the molten silicon and then slowly pulled out to create a solid crystal ingot.



2

A notch or flat is grounded into the ingot to provide orientation for the wafers. The ingot is then sawed into wafers, typically using a diamond blade.

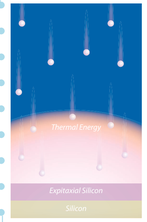
The wafers are rounded, and then polished to a mirror-like finish. Wafers are then cleaned and inspected for flatness and impurities.

3

Epitaxial silicon, a base layer of extremely pure silicon grown in a perfectly uniform crystalline structure, is used in some semiconductor devices to enhance device performance.

Epitaxial Silicon: $241.4 MN

1. ASMI: 36.7%
2. Applied Materials: 33.5%
3. LPE: 9.5%
4. Toshiba Machine: 7.3%
5. Moore Epitaxial: 7.0%



4

Oxidation is the process of growing silicon dioxide on the wafer. Silicon dioxide serves as an insulating layer, also known as a dielectric.

Oxidation/Diffusion Furnace: $5,814 MN

1. Tokyo Electron: 53.9%
2. Hitachi-Kokusai Elec.: 26.2%
3. Silicon Valley Group: 12.1%
4. ASM International: 6.1%
5. Koyo Lindberg: 0.9%

5

Photoresist, a light-sensitive material, is spun onto the wafer. Once developed, photoresist is etch resistant and helps to transfer an image of a mask onto the surface of the wafer.

A mask is placed above the wafer and UV light is flashed through the mask, exposing the resist.

Track: $2,237 MN

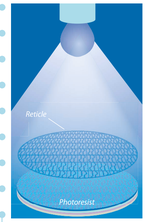
1. Tokyo Electron: 73.9%
2. Dainippon Screen: 16.1%
3. Silicon Valley Group: 4.3%
4. FSI International: 3.9%
5. Karl Suss: 1.5%

Mask Manufacturing: $295.6 MN

1. Applied Materials: 54.5%
2. Toshiba Machine: 16.3%
3. Hitachi: 12.7%
4. Micronic Laser Systems: 8.5%
5. JEOL: 4.6%

Stepper: $5,320.9 MN

1. Nikon: 36.7%
2. ASM Lithography: 34.6%
3. Canon: 20.6%
4. Silicon Valley Group: 6.8%
5. Ultratech Stepper: 1.3%



6

The Reticle (Mask) inspection tools use sophisticated image acquisition technology and image processing algorithms to capture the defects on the highly precise and sensitive reticles.

Reticle Inspection: $206.1 MN

1. KLA-Tencor: 76.2%
2. Lasertec Corp: 11.5%
3. Applied Materials: 6.3%
4. Carl Zeiss: 3.6%
5. Horiba Instruments: 2.4%

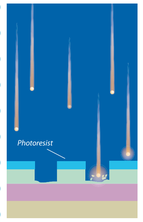
7

Etching removes the dielectric or conductive material below, leaving the pattern of the mask on the wafer.

A plasma etch process uses both chemical and physical means to etch away material off the wafer surface. Chemically reactive ions formed in the plasma react with the surface material, removing it and allowing it to be pumped away. Also, the plasma ions accelerate toward the wafer surface and physically sputter away the surface material.

Etch: $1,484.9 MN

1. Applied Materials: 34.2%
2. Lam Research: 29.1%
3. Tokyo Electron: 23.9%
4. Hitachi: 7.8%
5. Anelva: 1.3%

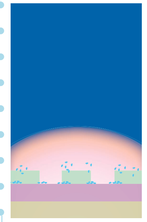


8

The remaining photoresist is removed by ashing. This patterning process is repeated many times during the wafer processing sequence.

Wet Stations: $1,372.7 MN

1. Dainippon Screen: 33.0%
2. Tokyo Electron: 14.5%
3. S.E.S. Co.: 11.9%
4. SCP Global Tech.: 10.8%
5. Kaijo Corp.: 10.6%



9

Ion Implantation is the process in which dopant ions are embedded into the wafer surface. In an implant tool, a focused beam of ionized dopant atoms is accelerated to a high enough speed to penetrate the wafer.

Implant: $1,672.8 MN

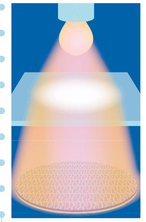
1. Axcelis: 38.6%
2. Varian: 38.1%
3. Applied Materials: 17.5%
4. Hitachi: 7.8%
5. Anelva: 1.3%

10

Annealing processes are often used to activate implanted ions and also to repair damage and smooth out rough surfaces on the wafer. Annealing can be done either in a batch furnace or in a single wafer Rapid Thermal Processing (RTP) chamber.

RTP: $631.1 MN

1. Applied Materials: 77.6%
2. Steag: 17.6%
3. Dainippon Screen: 2.5%
4. Axcelis: 0.9%
5. Ultratech Stepper: 0.6%



11

To deposit thin films of dielectric material on the wafer, Chemical Vapor Deposition (CVD) is typically used on more advanced devices. In a CVD process, gases are pumped into a heated chamber which react chemically and then form a thin film of the desired material onto the surface of wafer.

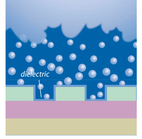
Some CVD chambers also use a plasma to generate highly reactive species to participate in the chemical reactions, thus speeding up the deposition process and achieving better surface coverage.

CVD: $4,898.3 MN

1. Applied Materials: 53.7%
2. Novellus: 22.5%
3. Tokyo Electron: 9.2%
4. ASM International: 3.5%
5. Hitachi-Kokusai Elec.: 3.5%

Spin-On Dielectric: $83.2 MN

1. Tokyo Electron: 48.4%
2. Tokyo Ohka Kogyo: 27.4%
3. Dainippon Screen: 14.1%
4. Semix: 10.2%



12

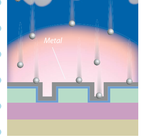
Metallization is the process of depositing a thin layer of metal on the wafer to form interconnects – electrical conducting paths that provide the electrical connections of the IC components.

Physical Vapor Deposition (PVD), also known as "sputtering," is typically used to lay down liners (Ti, TiN, TiW, TaN, etc.) and seed layers (Al, Cu). In the PVD process, an inert gas, such as argon, is introduced into an ultra-high vacuum chamber. A plasma is struck, and argon ions are accelerated into a target material, which is physically "sputtered" off and knocked onto the surface of the wafer.

CVD processes are typically used to fill contacts (W) and vias (W, Al, Cu) and deposit blanket metal films (Al, W).

PVD: $2,480.1 MN

1. Applied Materials: 82.1%
2. Ulvac: 6.8%
3. Anelva: 4.0%
4. Novellus: 2.3%

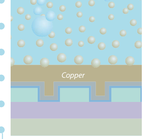


13

Copper is the newest conducting material being used for interconnects due to its low resistivity and resistance to electromigration. Copper fill is accomplished by Electro-Chemical Deposition (ECD), where the wafer surface is submerged in an electrically charged chemical bath (electrolytic plating bath). By applying a bias, the resulting chemical reaction deposits a thin film of Cu onto the surface of the wafer.

ECP: $159.6 MN

1. Novellus: 43.9%
2. Semitool: 31.3%
3. Applied Materials: 17.7%
4. Ebara: 5.3%
5. CuTek: 1.9%

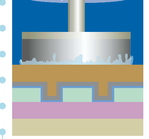


14

Chemical Mechanical Polishing (CMP) planarizes the wafer, ensuring a flat wafer surface before patterning, and also replacing certain etch steps. During CMP, a polishing head presses on a rotating wafer against a rotating abrasive pad. A wet chemical slurry containing a micro-abrasive is placed between the wafer and pad to ensure the wafer surface is smooth and flat.

CMP $1,649.5 MN

1. Applied Materials: 50.1%
2. Ebara: 19.8%
3. Speedfam: 13.9%
4. Lam Research: 9.2%

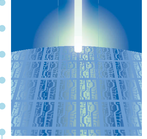


15

Scanning Electron Microscopes (SEMs) use an electron beam to image and measure a feature on a semiconductor wafer at a very high resolution. CD-SEMs measure the "critical dimensions," i.e., feature sizes of the chips, to assure the accuracy of the manufacturing process

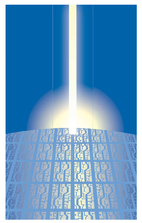
Process Control (Wafer Metrology, Inspection and Review): $3,703.2 MN

1. KLA-Tencor: 47.5%
2. Hitachi: 10.9%
3. Applied Materials: 9.3%
4. Therma-Wave: 4.5%
5. FEI: 3.6%



16

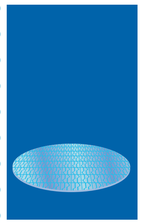
Defect Review (DF) SEMs identify and then classify defects on the wafer (such as particles, scratches or residue) to find sources of the defect.



17

The wafer processing sequence includes multiple steps of dielectric deposition, thermal processing, patterning, etching, metal deposition, CMP and wafer inspection.

At the end of the wafer processing sequences, a thin layer of nitride is deposited as a passivation layer to protect the underlying metal layers.

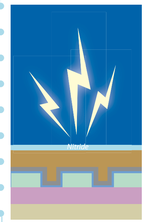


18

Wafer probing is the process in which the die on the wafer are checked to determine if it functions correctly. Wafers are placed onto a wafer prober, and pointed metal probes make contact with bonding pads and supply the necessary currents and voltages to the die under test. The die that function properly are left alone, and the die that fail are marked with a drop of ink.

Probers and Handlers: $937.6 MN

1. Tokyo Seimitsu Co.: 41.4%
2. Tokyo Electron: 28.2%
3. Electroglas: 20.4%
4. Karl Suss: 3.4%



19

The wafer is then held in place, and separated into die using a precision saw.

The die are then attached to the lead frame either by soldering the die by plating the back with gold or using a paste to glue the die to the lead frame.

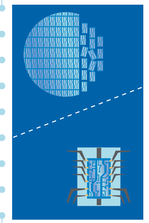
The next step is wire bonding, where the bonding pads on the die are connected to the lead frame by use of small gold wires.

Dicing Saws: $324.8 MN

1. Disco Corporation: 67.6%
2. Tokyo Seimitsu Co.: 19.0%
3. Machine Technology: 3.7%
4. Han-Mi Co.: 2.2%
5. Kulicke & Soffa: 2.2%

Wire Bonding: $1,411.1 MN

1. Kulicke & Soffa: 40.7%
2. Shinkawa Ltd: 20.3%
3. ASM Pacific: 18.1%
4. ESEC: 8.4%



20

The die are then packaged in a protective material to protect them against the environment, remove heat and allow for signals and power to be delivered to the chip.

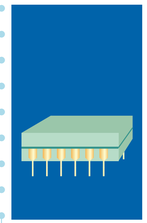
After packaging, the ICs go through a final test where run through several electrical and thermal tests to ensure quality of the ICs.

Molding/Encapsulation: $722.9 MN

1. TOWA Corp: 32.3%
2. Dai-Ichi Seiko: 29.0%
3. Apic Yamada: 16.0%
4. Be Semiconductor: 10.8%
5. Han-Mi Co.: 2.4%

Test (ATE)

1. TK
2. TK
3. TK
4. TK
5. TK



Analyst Name
(+1) xxx xxx xxxx
analyst.name@db.com

Analyst Name
(+1) xxx xxx xxxx
analyst.name@db.com

Deutsche Bank

Note: Objects not shown to scale. Processes have been simplified for the sake of visual clarity. Many of these steps are repeated hundreds of times to make a single chip. For added information, please contact your Deutsche Bank representative. For added amusement, keep in mind all processes are performed by people wearing bunny suits.

Trim line

trim line